DETAILED ACTION

1. Claims 21-42 are pending in the instant application.

Examiner's Remarks

2. The non-final office action filed January 23, 2008 failed to address the Applicant's new claims (41 and 42) filed December 3, 2007. Accordingly, this supplemental office action considers the additional claims 41 and 42 and restarts the time period for response.

Response to Amendment/Argument

3. With respect to the claim objections submitted in the office action dated July 20, 2007, the Applicant noted that "a clarification of the alleged informalities would be appreciated". Accordingly, the claim objections have been more specifically addressed.

4. The Applicant's remarks, filed December 3, 2007, have been considered by the Examiner. In view of the Applicant's remarks, new prior art rejections are set forth below.

5. The Applicant's amendment to claim 29 to overcome its rejection under 35 U.S.C. § 112, second paragraph, does not overcome the rejection. The rejection is clarified below.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 29 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 29, the claim is rejected because one skilled in the art is unable to determine a definite meaning for a "fractional proportion" of an address sequence. As commonly understood in the art, an address sequence consists of a number of address bits. The claim is indefinite because one is unable to determine how a fraction of a bit may be determined. Moreover, the Examiner suggests that the terms "high-value" and "low-value" are replaced with the more accepted language of "most-significant" and "least-significant" with respect to the address bits.

Claim Objections

8. Claims 21-40 are objected to because of the following informalities:

Regarding claim 21, the claim is objected to because one is unable to determine if the "correctional factors" (i.e. fig. 1, outputs from ASSIGNMENTS UNIT 4) and "new correctional values" are the same values. Following from figure 1, the "string of results" is generated during the "generating a string of results step" (i.e. via ADDITION/SUBTRACTION UNIT 7) and fed into the COMBINATION UNIT 8. Thereafter, in the "generating from the string of results" and "accumulating" steps, the claimed embodiment of the invention becomes confused with figure 1. Specifically, if, in figure 1, "d" represents a "generated string of results", the next "generating from the string of results step" which generates "new correctional values" and "output signals of the interpolation" becomes confused with the step of "accumulating" because the

"generated string of results" (i.e. "d") is only fed as input to the COMBINATION UNIT 8 for "accumulating" and can not create "correctional factors".

The following versions of claims 21 and 40 are presented by the Examiner to overcome objections to the claims.

21. A method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale, comprising:

converting each of the analog signals into a digital data stream by a sigma- delta modulator;

generating a string of results by combining the data streams with correctional ~~factors~~ values and subsequently combining the data streams with one another;

generating from the string of results ~~(a) new correctional values~~ a combination output in accordance with a quality criterion that is to be satisfied during interpolation ~~and (b) output signals of the interpolation~~;

accumulating over a specifiable time interval values of the ~~string of results~~ combination output for generating the correctional values and ~~the~~ output signals; and

using a signal sequence generated by the accumulation as an address sequence for generating the correctional values and for generating the output signals.

40. A device for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to each other and which are generated by scanning a measuring scale, comprising:

a sigma-delta modulator configured to convert the analog signals to a respective digital data stream;

an arithmetic unit configured to generate a string of results in accordance with a combination of the data streams with correctional ~~factors~~ values and ~~in accordance with~~ subsequent combination of the data streams with one another;

an arrangement configured to generate, from the string of results~~, (a) new correctional values~~ a combination output in accordance with a quality criterion that is to be satisfied during the interpolation ~~and (b) output signals of the interpolation~~;

a filter configured to accumulate values of the ~~string of results~~ combination output over a specified time interval to generate an address sequence to control the arithmetic unit to guide the string of results to satisfy the quality criterion; and

an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 21-24, 26, 27, and 30-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner (U.S. Pat. No. 5079549 – previously cited) in view of Garverick et al (U.S. Pat. No. 5134578; "Garverick" – previously cited).

Regarding claim 21, Liessner discloses a method for interpolating (col. 2, lines 20-25) at least two position-dependent, periodic analog signals (fig. 1, SIN(X), COS(X)) that are phase-shifted with respect to one another and which

are generated by scanning a measuring scale (abstract), comprising: generating a string of results (fig. 1, "ERROR SIGNAL") by combining (fig. 1, ref. 20) the periodic analog signals with correctional values (fig. 1, outputs of 16 and 18) and subsequently combining the periodic analog signals with one another; generating from the string of results (a) new correctional values (new or updated outputs of fig. 1, refs. 16 and 18) in accordance in accordance with a quality criterion (fig. 1, output of error "DETECTOR"; "ES>0" or "ES<0") that is to be satisfied during interpolation (col. 3, lines 40-55) and (b) output signals of the interpolation (fig. 1, "Y"); accumulating (fig. 1, ref. 24; fig. 4A, refs. 25 and 27) over a specifiable time interval (according to disable pulse generator, i.e. fig. 4A, ref. 29) values of the combination output for generating the correctional values (outputs of fig. 1, refs. 16 and 18) and output signals (fig. 1, "Y"); and using a signal sequence generated by the accumulation as an address sequence (also fig. 1, "Y") for generating the correctional values and for generating the output signals (fig. 1). Liessner discloses that the multipliers or combiners (fig. 1, refs. 12 and 14) which combine the periodic analog signals (fig. 1, SIN(X), COS(X)) with correctional values (fig. 1, outputs of 16 and 18) are "multiplying digital to analog converters that cause a digital input to attenuate an analog signal" (col. 3, lines 25-30). Therefore, the outputs from the lookup tables (fig. 1, refs. 16 and 18) are digital and the periodic signals (fig. 1, SIN(X), COS(X)) are analog ones which are attenuated according to the outputs from the lookup tables. Liessner does not explicitly disclose using sigma-delta modulators to convert the periodic analog

signals into digital signals. However, the use of digital data to represent analog waveforms is notoriously known in the art as evidenced by Garverick. The use of sigma-delta analog to digital converters is notoriously known in the art as evidenced by Garverick. Garcerick discloses the use of several sigma-delta analog to digital converters (fig. 1, refs. 21-26) to convert various phases of an analog signal into digital form (col. 4, lines 14-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the Liessner's "rotary or linear encoder" output (fig. 1, "SIN(X)" and "COS(X)") could be converted into digital form before being fed to multipliers (fig. 1, refs. 12 and 14) as suggested by Garverick. In the combination of Liessner in view of Garverick, Liessner's embodiment must be converted to a purely digital one. One skilled in the art would be enabled to complete the conversion with knowledge readily known in the art and motivated to complete the conversion because of the advantages provided by digital implementations of analog devices. Namely, proper digital implementations provide for zero loss in signal integrity as notoriously understood in the art.

Regarding claims 22 and 23, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, as broadly as claimed, Liessner's counter (fig. 1, ref. 24) is considered to be both a filter and an integrator because its output depends upon an accumulation of the past inputs.

Regarding claim 24, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses forming the address

sequence (fig. 1, "Y") from the accumulation (fig. 1, ref. 24), the address sequence including address values that represent phase information of the analog signals (col. 3, lines 35-40).

Regarding claim 26, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address values are a linear function of the phases of the periodic signals when the quality criterion is satisfied. The address values are a linear function of the phases because the error of phases directly determine the address values in a linear fashion (col. 4, lines 19-38).

Regarding claim 27, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address sequence (fig. 1, "Y") represent a phase value having a fractional proportion (col. 3, lines 35-40).

Regarding claim 30, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the generation of new correctional values is in accordance with the quality criterion (amount of error) until it is satisfied because the embodiment is a closed loop embodiment (fig. 1).

Regarding claim 31, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses storing possible correction values as predefined values in an assignment unit (col. 3, lines 35-40).

Regarding claim 32, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied in claim 21 above.

Regarding claim 33, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the correctional values correspond to values of a trigonometric function (col. 3, lines 35-40).

Regarding claim 34, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are phase shifted by 90 degrees with respect to each other as applied in claim 21 above.

Regarding claim 35, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are substantially sinusoid as applied in claim 21 above.

Regarding claim 36, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to multiplying (fig. 1, refs. 12 and 14).

Regarding claim 37, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, it is inherent that a piece of data may have a word width of one bit as understood by one having ordinary skill in the art.

Regarding claim 38, Liessner in view of Garverick disclose the limitations of claim 36 as applied above. Further, Liessner discloses the remaining

limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to reducing or attenuating (fig. 1, refs. 12 and 14; col. 3, lines 25-30; "attenuating").

Regarding claim 39, Liessner in view of Garverick disclose the limitations of claim 38 as applied above. Further, Liessner discloses combining by addition (fig. 1, ref. 20) the correctional values. Furthermore, in the purely digital implementation of Liessner in view of Garverick, the addition of the correctional values would result in one of four possibilities as understood by one having ordinary skill in the art because no other possibilities could exist.

Regarding claim 40, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

Regarding claim 41, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

Regarding claim 42, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above. Liessner in view of Garverick do not explicitly disclose an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation. However, Liessner discloses that "the digital output signal y is provided that *represents* displacement within a reticle cycle" (col. 2, lines 25-30). Because the digital output signal y only "represents" the displacement, it is obvious to one having ordinary skill in the art that an evaluation circuit would be required to convert the digital address value y into more useful information.

Moreover, Liessner suggests that the evaluation circuit may be a memory lookup table such as references 16 or 18 of figure 1 (col. 3, lines 35-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that an evaluation unit would be required to convert Liessner's y address values into a more useable format for their utility.

11. Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and in further view of The Applicant's Admitted Prior Art ("AAPA").

Regarding claim 25, Liessner in view of Garverick disclose the limitations of claim 24 as applied above. Liessner does not explicitly disclose that the output signals (fig. 1, "Y") are generated from the address sequence by low- pass filtering and assignment of the address values. However, low-pass filtering and assignment of the address values is well known in the art as evidenced in the discussion of the AAPA (page 2, lines 7-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the address sequence of Liessner could be fed through a low-pass filter (i.e. within UP/DOWN counter 26 of figure 1) as suggested by the AAPA because it was a well known method in the art.

12. Claims 28 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and Khan et al (U.S. Pat. Pub. 2002/0116181; hereafter "Khan" – newly cited).

Regarding claim 28, Liessner in view of Garverick disclose the limitations of claim 27 as applied above. Liessner in view of Garverick do not explicitly disclose that the correctional values are generated in the correctional value generating step in accordance with a high-value part and low-value part of the address sequence, the high-value part corresponding to an integer portion of the address values. However, Khan teaches an exemplary sine/cosine mapper according to figure 2 for determining from an upper two bits (input to 222) of the phase accumulation a quadrant in which a phase corresponding to the phase accumulation is located on an X-Y coordinate plane (para. 0055), a look-up table (226) for storing a predetermined number of sine or cosine values for one of four determined quadrants of the X-Y coordinate plane, and outputting a sine or cosine value (20 bits each "COS" and "SIN" output from 226) according to bits of the phase accumulation other than the upper two bits (i.e. "lower bits"; 18 remaining bits of 20 not fed into "OUTPUT SELECT" 222), and a cosine and sine value calculator (222) for calculating the sine and cosine values having phase corresponding to the phase accumulation according to the determined quadrant and the sine or cosine value received from the look-up table (paras. 0055-0058). Khan teaches the implementation of the mapper is effective and reduces overhead (para. 0010). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the sine/cosine lookup tables of Liessner (fig. 1, refs. 12 and 14) could be replaced

by the implementation taught by Khan because it is an effective method which reduces overhead.

Regarding claim 29, Liessner in view of Garverick disclose the limitations of claim 27 as applied above. Further, Liessner in view of Garverick, and Khan disclose the remaining limitations of the claim as applied to claim 28 above.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Jason M Perilla/
April 2, 2008

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/Chieh M Fan/

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